

1 CLAIMS:

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3 1. A method of forming a capacitor comprising:

4 forming a capacitor storage node having an uppermost surface and

5 an overlying insulative material over the uppermost surface;

6 after forming the capacitor storage node and the overlying

7 insulative material, forming a capacitor dielectric functioning region

8 discrete from the overlying insulative material operably proximate at least

9 a portion of the capacitor storage node; and

10 forming a cell electrode layer over the capacitor dielectric

11 functioning region and the overlying insulative material.

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13 2. The method of claim 1, wherein the forming of the capacitor

14 storage node comprises:

15 forming a layer of material over a substrate;

16 forming an opening received within the layer of material; and

17 forming a layer of conductive material within the opening to less

18 than fill the opening.

1 3. The method of claim 1, wherein the forming of the capacitor
2 storage node comprises:

3 forming a layer of material over a substrate;
4 forming an opening received within the layer of material;
5 overfilling the opening with conductive material; and
6 removing a sufficient amount of the conductive material to less
7 than fill the opening.

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9 4. The method of claim 1, wherein the forming of the capacitor
10 storage node comprises:

11 forming a layer of material over a substrate, the layer of material
12 having a generally planar outer surface; and
13 forming the storage node to be received within the layer of
14 material and to have an upper surface elevationally below the generally
15 planar outer surface.

1 5. The method of claim 1, wherein:

2 the forming of the capacitor storage node comprises:

3 forming a layer of material over a substrate;

4 forming an opening received within the layer of material; and

5 forming a layer of conductive material within the opening to

6 less than fill the opening; and

7 the forming of the insulative material comprises filling remaining
8 opening portions with the insulative material.

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10 6. The method of claim 1, wherein:

11 the forming of the capacitor storage node comprises:

12 forming a layer of material over a substrate, the layer of
13 material having a generally planar outer surface;

14 forming the storage node to be received within the layer of
15 material and to have an upper surface elevationally below the generally
16 planar outer surface; and

17 the forming of the insulative material comprises forming a
18 sufficient amount of the insulative material over the storage node to
19 have an insulative material surface which is generally coplanar with the
20 generally planar outer surface of the layer of material.

1 7. The method of claim 1, wherein:
2 the forming of the capacitor storage node comprises:
3 forming a layer of material over a substrate;
4 forming an opening received within the layer of material; and
5 forming a layer of conductive material within the opening to
6 less than fill the opening; and
7 prior to the forming of the capacitor dielectric function region,
8 etching the layer of material selectively relative to the insulative material
9 and exposing a side surface of the storage node.

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11 8. The method of claim 7 further comprising forming a layer
12 of roughened polysilicon over the exposed side surface of the storage
13 node.

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15 9. The method of claim 1 further comprising after the forming
16 of the cell electrode layer, conducting a maskless etch of the cell
17 electrode layer leaving cell electrode material only over generally vertical
18 surfaces.

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20 10. The method of claim 1, wherein the forming of the capacitor
21 storage node comprises forming said node as a capacitor storage node
22 container.

1 11. A method of forming a capacitor comprising:
2 forming a capacitor storage node having an uppermost surface and
3 a side surface joined therewith;
4 forming a protective cap over the uppermost surface;
5 forming a capacitor dielectric layer over the side surface and
6 protective cap; and
7 forming a cell electrode layer over the side surface of the
8 capacitor storage node.

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10 12. The method of claim 11, wherein the forming of the
11 capacitor storage node comprises:

12 forming a layer of material over a substrate;
13 forming an opening received within the layer of material; and
14 forming conductive material within the opening.

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16 13. The method of claim 11, wherein the forming of the
17 capacitor storage node comprises:

18 forming a layer of material over a substrate;
19 forming an opening received within the layer of material; and
20 filling the opening with conductive material.

1 14. The method of claim 11, wherein:

2 the forming of the capacitor storage node comprises:

3 forming a layer of material over a substrate;

4 forming an opening received within the layer of material; and

5 less than filling the opening with conductive material; and

6 the forming of the protective cap comprises forming the cap at
7 least within a remaining opening portion.

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9 15. The method of claim 11, wherein the forming of the
10 capacitor storage node comprises forming conductive material laterally
11 adjacent a layer of material, and further comprising after the forming
12 of the protective cap, removing material of the laterally adjacent layer
13 of material and exposing a side surface portion of the storage node.

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15 16. The method of claim 11, wherein the forming of the
16 capacitor storage node comprises forming conductive material laterally
17 adjacent a layer of material, and further comprising after the forming
18 of the protective cap, selectively etching material of the laterally adjacent
19 layer of material relative to the protective cap and exposing a side
20 surface portion of the storage node.

1 17. The method of claim 11, wherein the forming of the cell
2 electrode layer comprises forming the cell electrode layer over the
3 protective cap and storage node side surface, and removing material of
4 the cell electrode layer from over protective cap.

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6 18. The method of claim 11, wherein the forming of the cell
7 electrode layer comprises forming the cell electrode layer over the
8 protective cap and storage node side surface, and without a mask,
9 anisotropically etching the cell electrode layer.

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11 19. The method of claim 11, wherein:

12 the forming of the capacitor storage node comprises forming
13 conductive material laterally adjacent a layer of material, and further
14 comprising after the forming of the protective cap, removing material of
15 the laterally adjacent layer of material and exposing a side surface
16 portion of the storage node; and

17 the forming of the cell electrode layer comprises forming the cell
18 electrode layer over the protective cap and the storage node side surface
19 portion which was exposed, and anisotropically etching the cell electrode
20 layer.

1 20. The method of claim 11, wherein:

2 the forming of the capacitor storage node comprises forming
3 conductive material laterally adjacent a layer of material, and further
4 comprising after the forming of the protective cap, selectively etching
5 material of the laterally adjacent layer of material relative to the
6 protective cap and exposing a side surface portion of the storage node;
7 and

8 the forming of the cell electrode layer comprises forming the cell
9 electrode layer over the protective cap and the storage node side surface
10 portion which was exposed, and anisotropically etching the cell electrode
11 layer.

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13 21. The method of claim 11, wherein the forming of the
14 protective cap comprises forming said cap from insulative material.

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1 22. A method of forming a plurality of capacitors comprising:
2 forming a plurality of capacitor storage nodes arranged in columns;
3 forming a capacitor dielectric layer over at least portions of the
4 capacitor storage nodes;
5 forming a common cell electrode layer over the plurality of
6 capacitor storage nodes;
7 removing cell electrode layer material from between the columns
8 and isolating individual cell electrodes over individual respective capacitor
9 storage nodes; and
10 after the removing of the cell electrode layer material, forming
11 conductive material over portions of remaining cell electrode material and
12 placing some of the individual cell electrodes into electrical
13 communication with one another.

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15 23. The method of claim 22, wherein the forming of the
16 capacitor storage nodes comprises:
17 forming an insulative layer of material;
18 forming openings received within the insulative layer of material;
19 and
20 forming conductive material received within the openings.

1 24. The method of claim 22, wherein the forming of the
2 capacitor storage nodes comprises:

3 forming an insulative layer of material;

4 forming openings received within the insulative layer of material;

5 overfilling the openings with conductive material; and

6 removing portions of the conductive material and isolating the
7 capacitor storage nodes within the openings.

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9 25. The method of claim 22, wherein the forming of the
10 capacitor storage nodes comprises:

11 forming a first insulative layer of material;

12 forming openings received within the first insulative layer of
13 material;

14 overfilling the openings with conductive material;

15 removing portions of the conductive material to below an outer
16 surface of the first insulative layer of material;

17 forming a second different insulative layer of material at least
18 within remaining opening portions; and

19 removing material of the first insulative layer of material selectively
20 relative to material of the second insulative layer of material and
21 exposing a side surface of the conductive material.

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1 26. The method of claim 22, wherein the removing of the cell
2 electrode layer material comprises anisotropically etching the cell
3 electrode layer material.

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5 27. The method of claim 22, wherein the forming of the
6 conductive material over the remaining cell electrode material portions
7 comprises:

8 forming an insulative layer of material over the remaining cell
9 electrode material;

10 exposing at least some of the remaining cell electrode material
11 portions through the insulative layer; and

12 forming the conductive material over the remaining cell electrode
13 material portions.

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15 28. The method of claim 22, wherein the forming of the
16 conductive material over the remaining cell electrode material portions
17 comprises:

18 forming an insulative layer of material over the remaining cell
19 electrode material;

20 etching a trench into the insulative layer and exposing at least
21 some of the remaining cell electrode material portions; and

22 forming the conductive material within the trench.

1 29. The method of claim 22, wherein the forming of the
2 conductive material over the remaining cell electrode material portions
3 comprises:

4 forming an insulative layer of material over the remaining cell
5 electrode material;

6 etching a trench into the insulative layer and exposing at least
7 some of the remaining cell electrode material portions;

8 forming the conductive material within the trench; and

9 planarizing the conductive material within the trench relative to an
10 insulative layer outer surface.

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1 30. The method of claim 22, wherein:
2 the forming of the capacitor storage nodes comprises:
3 forming a first insulative layer of material;
4 forming openings received within the first insulative layer of
5 material;
6 overfilling the openings with conductive material;
7 removing portions of the conductive material to below an
8 outer surface of the first insulative layer of material;
9 forming a second different insulative layer of material at
10 least within remaining opening portions; and
11 removing material of the first insulative layer of material
12 selectively relative to material of the second insulative layer of material
13 and exposing a side surface of the conductive material; and
14 the removing of the cell electrode layer material comprises
15 anisotropically etching the cell electrode layer material.

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1 31. The method of claim 22, wherein:

2 the forming of the capacitor storage nodes comprises:

3 forming a first insulative layer of material;

4 forming openings received within the first insulative layer of

5 material;

6 overfilling the openings with conductive material;

7 removing portions of the conductive material to below an

8 outer surface of the first insulative layer of material;

9 forming a second different insulative layer of material at

10 least within remaining opening portions; and

11 removing material of the first insulative layer of material

12 selectively relative to material of the second insulative layer of material

13 and exposing a side surface of the conductive material; and

14 the forming of the conductive material over the remaining cell

15 electrode material portions comprises:

16 forming a third insulative layer of material over the

17 remaining cell electrode material;

18 exposing at least some of the remaining cell electrode

19 material portions through the third insulative layer; and

20 forming the conductive material over the remaining cell

21 electrode material portions.

1 32. The method of claim 22, wherein:

2 the forming of the capacitor storage nodes comprises:

3 forming a first insulative layer of material;

4 forming openings received within the first insulative layer of

5 material;

6 overfilling the openings with conductive material;

7 removing portions of the conductive material to below an

8 outer surface of the first insulative layer of material;

9 forming a second different insulative layer of material at

10 least within remaining opening portions; and

11 removing material of the first insulative layer of material

12 selectively relative to material of the second insulative layer of material

13 and exposing a side surface of the conductive material; and

14 the forming of the conductive material over the remaining cell

15 electrode material portions comprises:

16 forming a third insulative layer of material over the

17 remaining cell electrode material;

18 etching a trench into the third insulative layer and exposing

19 at least some of the remaining cell electrode material portions; and

20 forming the conductive material within the trench.

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1 33. A method of forming a plurality of capacitors comprising:
2 forming a plurality of capacitor storage nodes having respective
3 capacitor dielectric layers disposed thereover, the capacitor storage nodes
4 being arranged in columns;
5 forming a common cell electrode layer over the plurality of
6 capacitor storage nodes;
7 without masking, etching the common cell electrode layer to
8 electrically isolate individual cell electrodes over individual respective
9 capacitor storage nodes; and
10 electrically interconnecting selected electrically isolated individual
11 cell electrodes.

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13 34. The method of claim 33, wherein:
14 the forming of the capacitor storage nodes comprises forming
15 respective storage node upper surfaces and side surfaces joined therewith,
16 the respective side surfaces having first portions which are disposed
17 elevationally higher than an adjacent insulative material upper surface,
18 and second portions which are disposed elevationally lower than the
19 adjacent insulative material upper surface; and
20 the forming of the common cell electrode layer comprises forming
21 the layer laterally proximate the respective side surface first portions.

1 35. The method of claim 33 further comprising prior to the
2 forming of the common cell electrode layer, forming individual insulative
3 material caps over the capacitor storage nodes.

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5 36. The method of claim 33, wherein:

6 the forming of the capacitor storage nodes comprises forming
7 respective storage node upper surfaces and side surfaces joined therewith,
8 the respective side surfaces having first portions which are disposed
9 elevationally higher than an adjacent insulative material upper surface,
10 and second portions which are disposed elevationally lower than the
11 adjacent insulative material upper surface; and

12 after the forming of the capacitor storage nodes, forming individual
13 insulative material caps over the capacitor storage nodes' upper surfaces,
14 and wherein the forming of the common cell electrode layer comprises
15 forming the layer laterally proximate the respective side surface first
16 portions.

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1 37. The method of claim 33, wherein:
2 the forming of the plurality of capacitor storage nodes comprises:
3 forming an insulative layer;
4 forming individual storage nodes received within the insulative
5 layer; and
6 removing material of the insulative layer and partially
7 exposing respective storage node portions; and
8 the etching of the common cell electrode layer comprises forming
9 individual cell electrode bands around the node portions which were
10 previously exposed.

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1 38. The method of claim 33, wherein:

2 the forming of the plurality of capacitor storage nodes comprises:

3 forming an insulative layer;

4 forming individual storage nodes received within the insulative

5 layer;

6 forming protective caps over the capacitor storage nodes; and

7 selectively removing material of the insulative layer relative

8 to the protective caps and partially exposing respective storage node

9 portions; and

10 the etching of the common cell electrode layer comprises forming

11 individual cell electrode bands around the node portions which were

12 previously exposed and portions of the protective caps.

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1 39. A method of forming capacitor-over-bit line memory circuitry
2 comprising:

3 forming an opening in a first insulative material;
4 forming a conductive capacitor storage node within at least a
5 portion of the opening;

6 forming a second insulative material over the capacitor storage
7 node;

8 selectively removing portions of the first insulative material relative
9 to the second insulative material and exposing a portion of the
10 conductive capacitor storage node; and

11 forming a capacitor dielectric layer and a cell electrode layer
12 operably proximate the exposed portion of the conductive capacitor
13 storage node.

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15 40. The method of claim 39, wherein:

16 the forming of the conductive capacitor storage node comprises
17 partially filling the opening with conductive material; and

18 the forming of the second insulative material comprises filling a
19 remaining opening portion with second insulative material.

1 41. The method of claim 39, wherein:

2 the forming of the conductive capacitor storage node comprises
3 only partially filling the opening with conductive material; and

4 the forming of the second insulative material comprises filling a
5 remaining opening portion with second insulative material.

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7 42. The method of claim 39, wherein:

8 the forming of the conductive capacitor storage node comprises
9 partially filling the opening with conductive material;

10 the forming of the second insulative material comprises filling a
11 remaining opening portion with second insulative material; and

12 the removing of the portions of the first insulative material
13 comprise exposing a side surface of the storage node.

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15 43. The method of claim 39, wherein:

16 the removing of the portions of the first insulative material
17 comprises exposing a side surface of the storage node; and

18 the forming of the cell electrode layer comprises forming a band
19 of cell electrode layer material around the side surface which was
20 previously exposed.

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1 44. The method of claim 39, wherein:

2 the forming of the conductive capacitor storage node comprises
3 partially filling the opening with conductive material;

4 the forming of the second insulative material comprises filling a
5 remaining opening portion with second insulative material;

6 the removing of the portions of the first insulative material
7 comprises exposing a side surface of the storage node; and

8 the forming of the cell electrode layer comprises forming a band
9 of cell electrode layer material around the side surface which was
10 previously exposed.

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1 45. A method of forming capacitor-over-bit line memory circuitry
2 comprising:

3 forming a plurality of openings in a first insulative material;

4 less than filling the openings with a conductive material comprising
5 capacitor storage nodes;

6 filling the remaining openings with a second insulative material;

7 etching the first insulative material faster than any of the second
8 insulative material sufficient to expose portions of individual capacitor
9 storage nodes;

10 forming a capacitor dielectric layer and a common cell electrode
11 layer operably proximate portions of the conductive capacitor storage
12 nodes which were previously exposed;

13 anisotropically etching the common cell electrode layer and
14 isolating individual cell electrodes over individual respective capacitor
15 storage nodes; and

16 electrically interconnecting some of the isolated individual cell
17 electrodes with conductive material.

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19 46. The method of claim 45, wherein the less than filling of the
20 openings comprises overfilling the openings with the conductive material
21 and removing overfilled portions of the conductive material.

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1 47. The method of claim 45, wherein the etching of the common
2 cell electrode layer comprises forming respective bands around the
3 individual storage node portions which were previously exposed.

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5 48. The method of claim 45, wherein the interconnecting of the
6 isolated cell electrodes comprises:

7 forming a third insulative material over the isolated cell electrodes;
8 etching a trench into the third insulative material and exposing the
9 isolated individual cell electrodes; and
10 filling the trench with conductive material.

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12 49. The method of claim 45, wherein:

13 the etching of the common cell electrode layer comprises forming
14 respective bands around the individual storage node portions which were
15 previously exposed; and

16 the interconnecting of the isolated cell electrodes comprises:

17 forming a third insulative material over the isolated cell
18 electrodes;

19 etching a trench into the third insulative material and
20 exposing some of the band portions of the individual storage node
21 portions; and

22 filling the trench with conductive material.

1 50. A method of forming capacitor-over-bit line memory circuitry
2 comprising:

3 forming an array of storage nodes arranged into columns;
4 first electrically interconnecting the array of storage nodes in a
5 capacitor array configuration with a common cell electrode layer;

6 conducting a maskless etch within the array of the cell electrode
7 layer to remove selected portions thereof sufficient to isolate cell
8 electrodes over individual respective storage nodes; and

9 second electrically interconnecting some of the isolated cell
10 electrodes with conductive material.

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12 51. The method of claim 50, wherein the first electrically
13 interconnecting of the array of storage nodes comprises forming the
14 common cell electrode layer over and laterally proximate the storage
15 nodes.

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17 52. The method of claim 50, wherein the conducting of the
18 maskless etch comprises anisotropically etching the cell electrode layer.

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20 53. The method of claim 50, wherein the conducting of the
21 maskless etch comprises forming a band of cell electrode layer material
22 around portions of the respective storage nodes.

1 54. The method of claim 50, wherein the forming of the array
2 of storage nodes comprises forming insulative caps over and not laterally
3 proximate conductive material comprising the storage nodes.

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5 55. The method of claim 50, wherein:

6 the forming of the array of storage nodes comprises forming
7 insulative caps over and not laterally proximate conductive material
8 comprising the storage nodes; and

9 the conducting of the maskless etch comprises forming a band of
10 cell electrode layer material around portions of the respective storage
11 nodes and portions of their associated insulative caps.

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13 56. A method of forming a series of capacitors comprising
14 forming a plurality of first and second capacitor electrode layers
15 separated by intervening dielectric layers, one of the first and second
16 capacitor electrode layers being formed, at least in part, by conducting
17 a maskless anisotropic etch of conductive material comprising the one
18 layer.

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20 57. The method of claim 56, wherein the conducting of the
21 anisotropic etch comprises forming a band comprising conductive material
22 of the one layer around conductive material of the other layer.

1 58. The method of claim 56 further comprising forming a
2 protective cap of material over the other of the layers prior to
3 conducting the maskless anisotropic of the conductive material comprising
4 the one layer.

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6 59. The method of claim 56 further comprising forming a
7 protective cap of material over the other of the layers prior to
8 conducting the maskless anisotropic of the conductive material comprising
9 the one layer, and wherein the conducting of the anisotropic etch
10 comprises forming a band comprising conductive material of the one
11 layer around conductive material of the other layer.

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13 60. Integrated circuitry comprising:

14 a capacitor storage node having an uppermost surface and a side
15 surface joined therewith;
16 a protective cap over the uppermost surface;
17 a capacitor dielectric layer over the side surface; and
18 a cell electrode band disposed proximate at least a portion of the
19 storage node side surface and not over the storage node uppermost
20 surface.

1 61. The integrated circuitry of claim 60, wherein the protective
2 cap has a side surface, and the cell electrode band is disposed laterally
3 proximate at least a portion of the protective cap side surface.

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5 62. The integrated circuitry of claim 60, wherein the cell
6 electrode band is disposed over less than an entirety of the storage node
7 side surface.

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9 63. The integrated circuitry of claim 60, wherein the cell
10 electrode band has an uppermost portion which extends elevationally
11 higher than any material of the capacitor storage node.

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13 64. The integrated circuitry of claim 60, wherein:
14 the protective cap has a side surface, and the cell electrode band
15 is disposed laterally proximate at least a portion of the protective cap
16 side surface; and
17 the cell electrode band has an uppermost portion which extends
18 elevationally higher than any material of the capacitor storage node.

65. The integrated circuitry of claim 60, wherein:

- 1 the cell electrode band is disposed over less than an entirety of
- 2 the storage node side surface; and
- 3 the cell electrode band has an uppermost portion which extends
- 4 elevationally higher than any material of the capacitor storage node.

7 66. Integrated circuitry comprising:

8 a capacitor storage node having an uppermost surface;

9 an insulative material overlying the uppermost surface;

10 a capacitor dielectric functioning region discrete from the overlying

11 insulative material and disposed operably proximate at least a portion of

12 the capacitor storage node; and

13 a cell electrode layer disposed laterally proximate the capacitor

14 dielectric functioning region and the overlying insulative material.

16 67. The integrated circuitry of claim 66, wherein a substantial
17 portion of the dielectric functioning region is disposed only laterally
18 proximate the capacitor storage node.

1 68. The integrated circuitry of claim 66, wherein the dielectric
2 functioning region comprises a layer of dielectric material which extends
3 over the overlying insulative material and defines a non-dielectric
4 functioning region.

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6 69. The integrated circuitry of claim 66, wherein the dielectric
7 functioning region defines a band of dielectric material which laterally
8 encircles at least a portion of the storage node.

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10 70. The integrated circuitry of claim 66, wherein the cell
11 electrode layer defines a band of conductive material which laterally
12 encircles at least a portion of the storage node.

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14 71. The integrated circuitry of claim 66, wherein the cell
15 electrode layer defines a band of conductive material which laterally
16 encircles at least a portion of the storage node and comprises an
17 uppermost band portion which extends elevationally higher than the
18 storage node uppermost surface.

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1 72. A capacitor-over-bit line memory array comprising:

2 a substrate;

3 a pair of spaced-apart conductive lines disposed over the substrate;

4 a pair of diffusion regions received within the substrate operably

5 proximate the conductive lines;

6 conductive material disposed over and in electrical communication

7 with the diffusion regions, the conductive material extending away from

8 the diffusion regions;

9 a pair of capacitor storage nodes, each of which being operably

10 joined with and in electrical communication with a respective one of the

11 diffusion regions through the conductive material disposed thereover, each

12 storage node having an uppermost surface and a side surface joined

13 therewith;

14 a protective cap over each uppermost surface;

15 a capacitor dielectric layer over each side surface; and

16 a cell electrode band disposed proximate at least a portion of each

17 storage node side surface and not over the associated storage node

18 uppermost surface.

1 73. The capacitor-over-bit line memory array of claim 72, wherein
2 each protective cap has a side surface, and the cell electrode band
3 associated therewith is disposed laterally proximate at least a portion of
4 the protective cap side surface.

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6 74. The capacitor-over-bit line memory array of claim 72, wherein
7 each cell electrode band is disposed over less than an entirety of its
8 associated storage node side surface.

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10 75. The capacitor-over-bit line memory array of claim 72, wherein
11 each cell electrode band has an uppermost portion which extends
12 elevationally higher than any material of its associated capacitor storage
13 node.

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15 76. The capacitor-over-bit line memory array of claim 72,
16 wherein:

17 each protective cap has a side surface, and the cell electrode band
18 associated therewith is disposed laterally proximate at least a portion of
19 the protective cap side surface; and

20 each cell electrode band has an uppermost portion which extends
21 elevationally higher than any material of its associated capacitor storage
22 node.

1 77. The capacitor-over-bit line memory array of claim 72,
2 wherein:

3 each cell electrode band is disposed over less than an entirety of
4 its associated storage node side surface; and

5 each cell electrode band has an uppermost portion which extends
6 elevationally higher than any material of its associated capacitor storage
7 node.

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